We study the application of error correcting codes in the design of demultiplexers used on the interface between micro- and nano-electronic circuits. The cases of diode and resistor-based demultiplexers are considered. The analysis of the diode-based application leads to new formulas for error probability that are hybrids of the erasure and full error correction cases in conventional ECC. A notion of "coding gain" can be defined, that is analogous to the one used in conventional communication applications, but applies to manufacturing cost. In the resistor-based case, the engineering requirements translate to a combinatorial constraint that seeks to minimize the ratio between the maximum and minimum distances of the code. We present examples of (nonlinear) optimal codes for practical circuit sizes currently in development by nanotech researchers.

The talk summarizes work done at HP Labs jointly with Ronny Roth, Phil Kuekes, Warren Robinett, and Stan Williams.